FULL PAPER

Nonvolatile Floating-Gate Memories Based on Stacked Black Phosphorus–Boron Nitride–MoS_2 Heterostructures

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Research on van der Waals heterostructures based on stacked 2D atomic crystals is intense due to their prominent properties and potential applications for flexible transparent electronics and optoelectronics. Here, nonvolatile memory devices based on floating-gate field-effect transistors that are stacked with 2D materials are reported, where few-layer black phosphorus acts as channel layer, hexagonal boron nitride as tunnel barrier layer, and MoS_2 as charge trapping layer. Because of the ambipolar behavior of black phosphorus, electrons and holes can be stored in the MoS_2 charge trapping layer. The heterostructures exhibit remarkable erase/program ratio and endurance performance, and can be developed for high-performance type-switching memories and reconfigurable inverter logic circuits, indicating that it is promising for application in memory devices completely based on 2D atomic crystals.

1. Introduction

Since the successful isolation of graphene from bulk graphite,[1] 2D atomic crystals have involved into a vast field in many topics and are proposed to be widely applied in electronics,[2,3] optoelectronics,[4–6] spintronics,[7] and flexible and transparent devices.[8,9] So far, various 2D materials, including conductors (such as graphene), semiconductors (such as MoS_2), and insulators (such as h-BN), have been well studied and exhibit prominent properties. Stacking these 2D crystals layer by layer into van de Waals heterostructures provides an effective way to design novel artificial materials with remarkable characteristics by utilizing special properties of each component.[10,11] Therefore, the emergence of such heterostructures opens one possible way to fabricate high-performance new device structures.[12–17]

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Floating-gate field-effect transistors (FGFETs), operated with multiple functional units of control gate, dielectric, charge trapping, potential barrier, and field-effect transistor (FET) channel layer, can be developed for nonvolatile memory devices. Previous studies indicate that graphene or MoS_2 could be engaged into the structures to produce nonvolatile memories.[18–23] By using hexagonal boron nitride (h-BN) as barrier layer, stacked graphene/h-BN/MoS_2 memories were also developed, and MoS_2 and h-BN have been proved to be an effective charge trapping and potential barrier layer, respectively.[24] Based on the ambipolar FET behavior, graphene could also be used for ambipolar memory devices that could serve as type-switching memories and inverter logic circuits. However, their properties are limited by the zero bandgap of graphene.[25] In order to get high-performance nonvolatile ambipolar memories, semiconducting ambipolar FET channel should be explored. Recently, FETs based on semiconducting few-layer black phosphorous (BP) flakes show an ambipolar characteristic with high on/off ratio exceeding up to 10^5 and prominent charge carrier mobility up to 1000 $cm^2\ V^{-1}\ s^{-1}$.[26] It thus arouses widespread attention and has been widely exploited for electronics and optoelectronics.[27–29] By using BP flakes as FET channels, here we designed BP/h-BN/MoS_2 stacked heterostructures and found that they could be developed for high-performance nonvolatile memories and inverter logic circuits.

2. Results and Discussion

The configuration of the designed BP/h-BN/MoS_2 heterostructure FGFET memory devices is schematically demonstrated in **Figure 1**a, where highly doped n-type Si serves as control gate electrode. MoS_2, h-BN, and BP flakes are all produced with a mechanical exfoliation method. In the device structure, a piece of MoS_2 flake is first transferred on the 300 nm thick thermal oxide film, which acts as a charge trapping layer (floating gate). H-BN and BP flakes are then aligned on the MoS_2 flake successively, which are employed as a potential barrier and an FET channel layer, respectively. The device fabrication details can be seen in Experimental Section, which is mainly accomplished with a dry transfer process and the standard e-beam lithography (EBL) method.

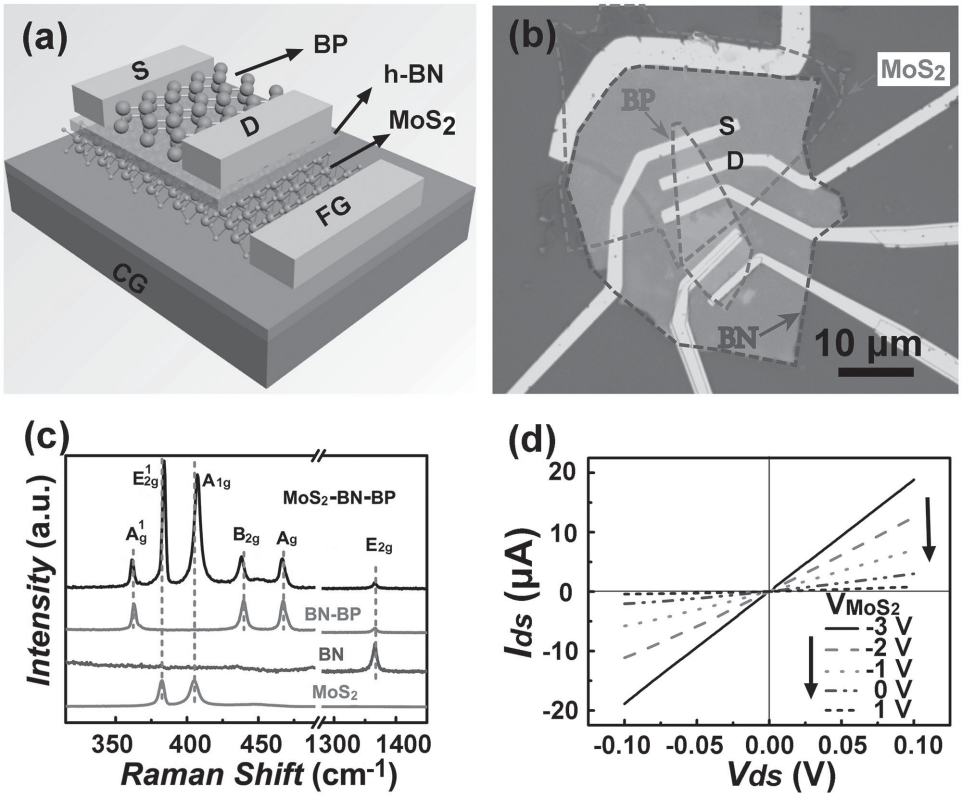

Figure 1. FGFET memory device configuration based on stacked BP/h-BN/MoS_2 heterostructures. a) Schematic of the BP/h-BN/MoS_2 sandwich FGFET device structure. A highly n-doped Si wafer (as control gate) with 300 nm SiO_2 (as gate dielectric) is used as the substrate. BP, h-BN, and MoS_2 are engaged as the FET channel, tunnel barrier, and floating gate, respectively. b) Optical micrograph of a typical fabricated device. The dotted lines indicate the boundary of each material. The BP/h-BN/MoS_2 overlapped region indicates an FGFET device (*device 1*). The BP/h-BN overlapped region indicates an FET device (*device 2*). c) Raman spectra of the BP, h-BN, MoS_2, and the overlapped region. Raman signatures of each component are observed in the overlapped region. d) I_{ds}–V_{ds} curves across the BP flake recorded at different voltages applied on the MoS_2 gate electrode.

Figure 1b shows an optical microscopy image of a typical BP/h-BN/MoS_2 engaged device. Boundary of each component is highlighted by dotted line with different colors. The BP/h-BN/MoS_2 overlapped region presents an FGFET device (*device 1*), and the BP/h-BN overlapped region indicates an FET device (*device 2*). The thickness of each component is determined by atomic force microscopy (AFM) and the results are shown in Figure S1 (Supporting Information), exhibiting that the BP, h-BN, and MoS_2 flakes are all few-layer structures with the thickness of 8, 25, and 6 nm, respectively.[1,24,26] To confirm the presence of the components, Raman spectroscopy measurements were performed. The Raman signatures of MoS_2 (E_{2g}^1 peak at 383 cm^{-1} and A_{1g} peak at 408 cm^{-1}),[30] h-BN (E_{2g} peak at 1366 cm^{-1})[31] and BP (A_g^1 peak at 365 cm^{-1}, B_{2g} peak at 440 cm^{-1}, and A_g^2 peak at 470 cm^{-1})[32,33] are clearly observed in the MoS_2/h-BN/BP heterostructure device (Figure 1c).

The electrical behaviors of the devices were characterized in vacuum at room temperature. The FET characteristics of *device 1* were first measured by using the MoS_2 layer as gate electrode and the h-BN as dielectric. Figure 1d shows the I_{ds}–V_{ds} (current vs bias voltage) curves across the source and drain recorded at different gate voltages. The results demonstrate that the currents are linearly dependent on the bias voltages, indicating that the Au/Cr electrodes form Ohmic contact to the few-layer BP flake. As shown in the inset in **Figure 2**a, its transfer characteristic curve demonstrates a small hysteresis. It should be due to the interfacial charge trapping states. The mobility is estimated to be ≈430 cm^2 V^{-1} s^{-1}, which is close to the reported results, indicating that the BP/h-BN/MoS_2 structure should be a considerable candidate for BP FETs.[26]

We further measured the transfer characteristics of the BP/h-BN/MoS_2 engaged heterostructure device displayed in Figure 1b (*device 1*), where the bias voltage across the source and drain is fixed at 50 mV. We first sweep the Si control gate voltage from −40 to +40 V. The transfer characteristic curve exhibits a large negative shift of the lowest conductance point (Dirac point) compared to the normal BP FET that is often in the positive gate voltage region due to its p-type intrinsic property (see Figure 2a; Figure S2, Supporting Information).[26] Moreover, it presents a pretty large voltage hysteresis (ΔV) of ≈60 V while the sweeping direction of the control gate voltage is reversed from +40 to −40 V. The large voltage hysteresis is obviously different from the above discussed BP/h-BN/MoS_2 FET, where the MoS_2 serves as a gate electrode. In comparison, the BP/h-BN structured device is characterized in the same way by using Si as a gate electrode (*device 2* in Figure 1b). The results displayed in Figure S2 (Supporting Information) show typical BP-engaged FET transfer curves with a small hysteresis too. Thus, it can be concluded that the presence of the large voltage hysteresis is attributed to the existence of the MoS_2 interlayer

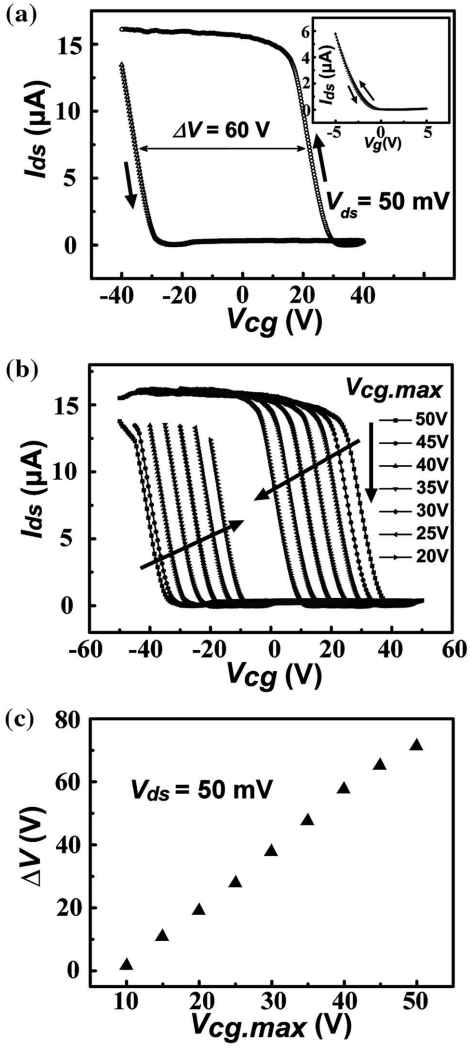

Figure 2. FGFET device characterizations. a) Transfer characteristic curves (drain-source current I_{ds} vs control gate voltage V_{cg}) of *device 1*, which includes two sweep directions (from −40 to +40 V in the positive direction and +40 to −40 V in the negative direction) denoted with blue curve and red curve, respectively. The inset shows the transfer characteristic curves of *device 1* with the MoS_2 as the gate electrode. b) Memory windows in accordance with different control gate voltage scanning ranges. c) Variation of the hysteresis voltage (memory window width, ΔV) dependent on the maximum control gate voltage ($V_{cg,max}$).

between the Si control gate and BP FET channel. The mechanism is to be discussed later.

Such large voltage hysteresis observed in the BP/h-BN/MoS_2 heterostructured FGFETs can be used for nonvolatile memory devices, where the BP, h-BN, MoS_2, and Si act as FGFET charge transport channel, tunneling barrier, floating gate, and control gate, respectively. We now probe the storage capability of the memory devices. It is strongly dependent on the memory window demonstrated in Figure 2a. A larger memory window means that the memory device is more reliable. While the control gate voltage is swept from −40 to +40 V and back to −40 V, the device presents a large memory window of ≈60 V. Moreover, the memory window can be modulated by varying the voltage scanning range applied on the Si control gate. Figure 2b shows the obtained memory windows with different voltage scanning ranges, and Figure 2c demonstrates the memory window width dependent on the maximum control voltage (ΔV vs $V_{cg,max}$). The results indicate that the width of the memory window is gradually enlarged with the maximum control gate voltage increasing. The $V_{cg,max}$ of 50 V can even get a ΔV over 70 V, and the $V_{cg,max}$ of 15 V can reach over 15 V. The excellent storage capability of our memory devices should be due to the remarkable properties of the composed layered materials. **Figure 3** exhibits the operating mechanism of the BP/h-BN/MoS_2 engaged memory devices. Few-layer MoS_2 has a bandgap of ≈1.2 eV and an electron affinity of ≈4.0 eV, which has been proved to be an effective charge storage layered material.[24,34] For few-layer BP, they are ≈0.3 and ≈4.1 eV, respectively.[26,35] On the contrary, h-BN has a large bandgap (5.2–5.9 eV) and a small electron affinity (2–2.3 eV).[24] It indicates that the h-BN can act as an effective potential barrier to hold the charges in the MoS_2 layer. While a negative voltage is applied on the control gate, holes are induced in the BP channel due to the electrical field effect and can tunnel through the h-BN from the BP to the MoS_2 layer. The accumulation of holes in the MoS_2 layer screens the electric field from the control gate to the BP channel, leading to a negative shift of the threshold voltage (blue curve in Figures 2a and 3b). With the control gate swept to the positive voltage, the tunneled holes would be drawn back. It should be noted here that BP has an especial property similar to graphene, whose charge carrier dominant-type and density can be modulated by external electrical field. Therefore, while the control gate voltage is in the high positive region, electrons would be dominated in the BP and can tunnel into the MoS_2 layer, resulting in a positive shift of the threshold voltage (red curve in Figures 2a and 3c). Figure S3 (Supporting Information) shows the transfer curves of the device with the control gate first swept from +40 to ≈40 V and then back to + 40 V. They are almost similar to the curves with −40 to +40 V and then back to −40 V. It confirms that electrons can also be tunneled and stored in the MoS_2 layer. This is different from the reported memory device structures and should be responsible to the pretty large memory windows demonstrated in our memory device.[24] The results also indicate that the heterostructures here should be further developed for ambipolar memory devices.[25]

The amount of charges stored in the MoS_2 trapping layer (floating gate) can be estimated by the equation of $n = (\Delta V \times C_{cg-fg})/e$, where e is the electron charge, ΔV is the threshold voltage shift, $C_{cg\text{-}fg} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{d_{SiO_2}}$ is the capacitance between the control gate and floating gate, with ε_0 the vacuum permittivity, and ε_{SiO2} and d_{SiO2} the relative dielectric constant (≈3.9) and thickness (300 nm) of the SiO_2, respectively.[22] Based on this equation, the density of the stored holes and electrons is estimated to be on the order of 10^{12} cm^{-2}, which is close to the reported results by employing SiO_2 as dielectric for control gate, but a little smaller compared with h–κ materials.[22–24] If h–κ dielectric is used, memory devices of such heterostructures with even better performance should be expected.

The retention characteristics of the program/erase state are crucial for nonvolatile memory devices. As shown in **Figure 4**a, the bias voltage across the source and drain is fixed at 50 mV.

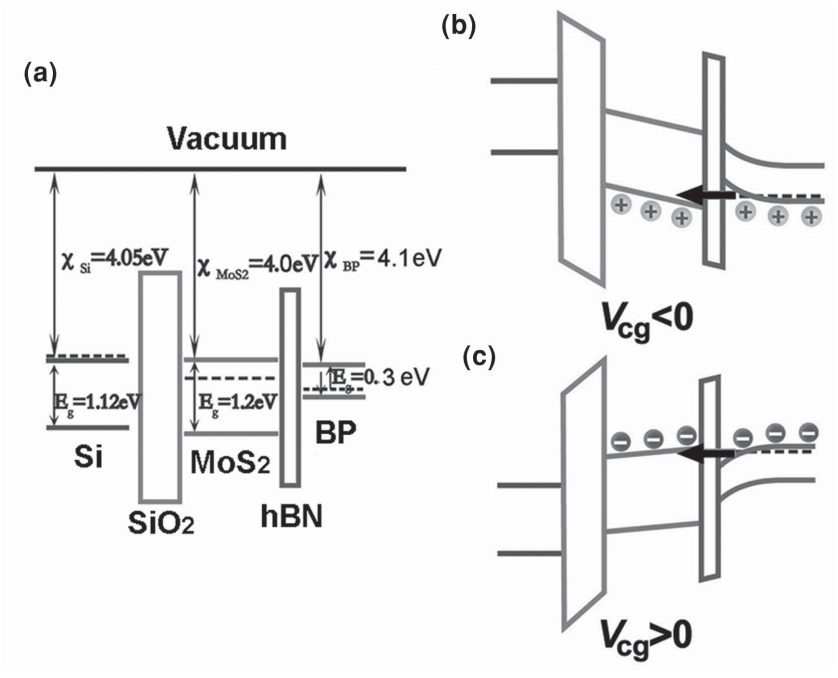

Figure 3. Charge trapping mechanism of the BP/h-BN/MoS_2 heterostructure device. a) Flat energy band structure, where χ and E_g represent the electron affinity and bandgap of semiconductors, respectively. b) Schematic energy band diagram of the FGFET at the program ("Off", negative control gate voltage) state, and c) erase ("On", positive control gate voltage) state.

After a positive voltage pulse (+20 V, 300 ms) applied on the control gate, electrons are accumulated in the MoS_2 floating-gate layer. When the control gate voltage is reset to 0 V, the memory remains on the erase ("On") state. For program ("Off") state, the retention performance is carried out with a negative voltage pulse (–20 V, 300 ms). The results exhibit that the erase/program ratio is ≈50. After 1000 s, the erase state current is slowly weakened from 1.20×10^{-5} to 1.16×10^{-5} A, and the program state is varied from 2.65×10^{-7} to 2.36×10^{-7} A, indicating that the device demonstrates a pretty good retention behavior.

Figure 4b shows the dynamic performance of the device with a bias voltage of 50 mV, exhibiting that the device can be switched between the program and erase state by applying negative (positive) voltage pulse to the control gate electrode. The device is initially on the program ("Off") state by applying a 300 ms voltage pulse of –20 V to the control gate. While the control gate voltage is reset to 0 V, the device still works on the program state. A 300 ms voltage pulse of +20 V can rapidly switch the device to the erase ("On") state. And the device can remain on the erase state until a –20 V voltage pulse applied. The endurance performance measurement of the device is shown in Figure 4c. After 40 switching cycles, the device is still very stable.

As demonstrated above, both of holes and electrons can be stored in the MoS_2 charge trapping layer and the BP exhibits ambipolar behavior, indicating that the BP/h-BN/MoS_2 heterostructure-based memories can be developed for type-switching memories and reconfigurable inverter logic circuits.[25] **Figure 5**a shows a hysteresis curve of a BP/h-BN/MoS_2 heterostructure with a voltage scanning range between –13 and 10 V. As shown in Figure 5a, the curve with a forward sweeping direction from –13 to 10 V indicates that the BP is n-type in the rectangle range, and the curve with a reverse sweeping direction from 10 to –13 V exhibits that the BP is p-type in the rectangle range. It means that a –13 V pulse applied on the control gate can make the device with an n-type channel while it works at low control gate voltages in the rectangle. On the contrary, a 10 V pulse makes it for p-type. This behavior can be used to develop type-switching memories. Here, we used a similar method as reported to monitor the type-switching memory behavior of the BP/h-BN/MoS_2 heterostructure based devices.[25] As shown in Figure 5b, while a large positive 10 V voltage is first applied on the control gate, electrons are charged in the MoS_2 layer. After that, a small sinusoidal voltage (between –1 and 1 V) is applied on the control gate. The result exhibits that the current across the BP channel decreases with the gate voltage increasing, indicating a p-type behavior, and a large negative –13 V voltage applied on the control gate can switch the device to n-type, where the current increases with the gate voltage increasing.

The BP/h-BN/MoS_2 heterostructure memory was also developed for reconfigurable inverter logic circuit, where a 1 MΩ resistor is connected between the source and the ground, and a 1 V bias (V_{DD}) is applied on the drain (as shown in Figure 5c). While a large positive voltage pulse (10 V) is applied on the control gate, electrons are charged in the MoS_2 layer and the memory is then working at a p-type mode. At this situation, the output voltage (V_{out}) decreases with the control gate voltage (V_{in}) increasing just as an inverter. However, while a large negative voltage pulse (–13 V) is applied on the control gate, the memory is then working at an n-type mode. At this situation, the V_{out} increases with V_{in} increasing, indicating that the inverter behavior disappears. It should be noted here that the BP/h-BN/MoS_2 heterostructure exhibits much better behavior than graphene oxide (GO)-based ambipolar memories whatever it serves as type-switching memories or reconfigurable inverter logic circuits. For type-switching memories, GO exhibits a poor on/off ratio less than 1% with the control gate voltage varied from –1 to 1 V, and for inverter, the V_{out} variation of GO devices is only from ≈1.03 to ≈1.02 V.[25] However, our device exhibits a pretty large type-switching memory on/off ratio ≈100 and a much better V_{out} variation from ≈0.77 to ≈0.45 V, which is obviously ascribed to the large on/off ratio of BP-based ambipolar FETs.

3. Conclusions

In conclusion, we have thus demonstrated nonvolatile memory devices based on stacked BP/h-BN/MoS_2 heterostructures on SiO_2 dielectric. Owing to the excellent properties of the composed layered materials, the device exhibits a pretty large memory window as high as ≈60 V for maximum control gate voltage of 40 V, and it can be modulated by varying the

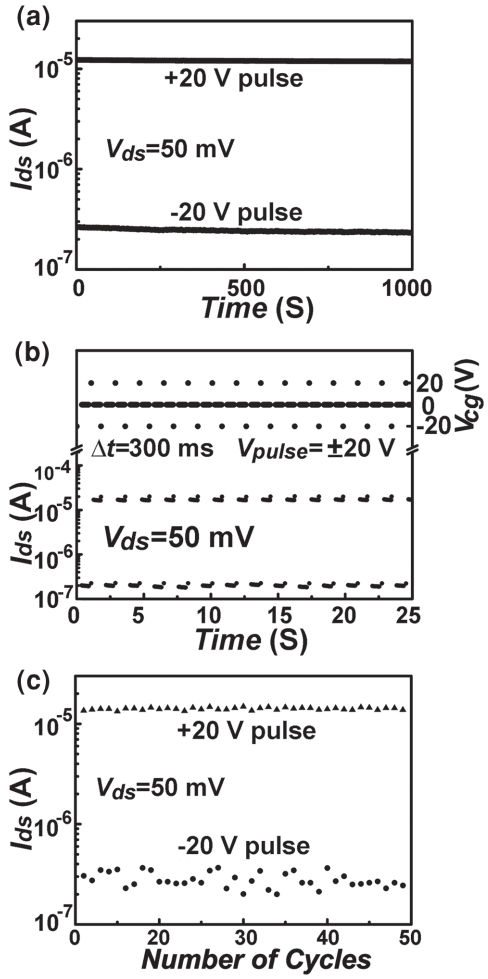

Figure 4. Memory dynamic characteristics of the BP/h-BN/MoS_2 heterostructure device (*device 1*). a) Retention performance. The current is measured at V_{cg} = 0 V with pulse of +20 V and −20 V, pulse width of 300 ms and V_{ds} of 50 mV. The high- and low-current levels correspond to the erase ("On") state and program ("Off") state, respectively. b) Switching behavior between the erase and program states. The measurement is carried out with V_{ds} of 50 mV and V_{cg} of 0 V by alternately applying voltage pulse (+20 and −20 V) to the control gate. c) Endurance of the memory device for 40 cycles with V_{ds} of 50 mV, erase/program voltage pulse of +20 V/−20 V and pulse width of 300 ms.

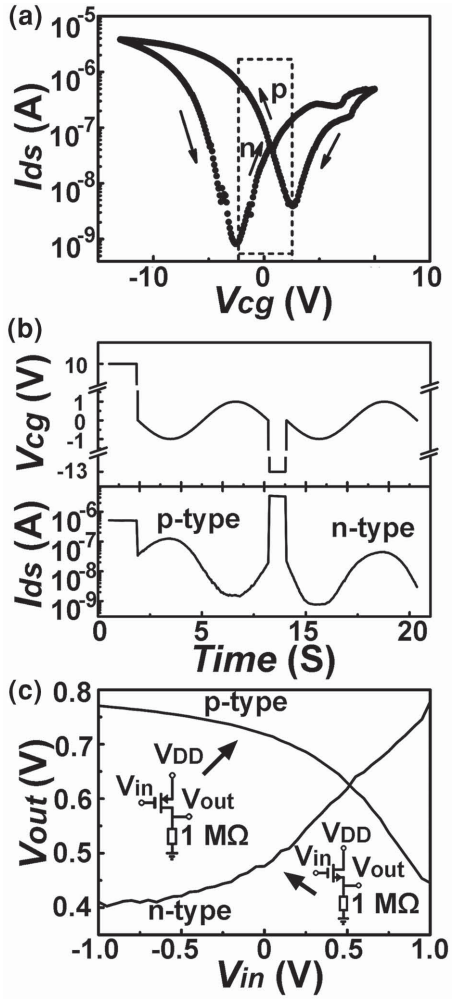

Figure 5. Type-switching memory and reconfigurable inverter logic circuit characterization of BP/h-BN/MoS_2 heterostructure-based devices. a) A typical hysteresis curve measured at a drain voltage of 50 mV with the control gate voltage swept from −13 to +10 V and back to −13 V, exhibiting both n- and p-type characteristics near zero gate voltage in the indicated rectangle. b) Type-switching memory behavior characterization. After a 10 V voltage pulse, the memory works at a p-type mode at low gate voltages and exhibits a 180° phase shift between the input signal and the output signal. A −13 V voltage pulse can effectively switch the memory to an n-type mode. c) Output characteristics of the reconfigurable inverter that includes a memory and a 1 MΩ resistor. The curves correspond to the p-type mode (with 10 V pulse) and n-type mode (with −13 V pulse).

maximum control gate voltage. Electrons and holes can be stored in the MoS_2 charge trapping layer due to the ambipolar behavior of few-layer black phosphorus, and the BP/h-BN/MoS_2 heterostructures can be developed for high-performance type-switching memories and reconfigurable inverter logic circuits. Combining the high erase/program ratio, excellent charge storage and endurance, it indicates that it is promising to design flexible and transparent high-performance memory devices totally based on 2D layered materials.

4. Experimental Section

BP/h-BN/MoS_2 Heterostructure Engaged Memory Devices Fabrication: The device fabrication process is schematically demonstrated in Figure S4 (Supporting Information). Few-layer BP, h-BN, and MoS_2 flakes were all produced with a mechanical exfoliation method from bulk crystals. They were aligned on highly doped silicon wafers with a 300 nm thick thermal oxide film. The assembly of the few-layer flakes was processed with a dry transfer procedure as reported.[36] Typically, a few-layer MoS_2 flake was first transferred on the Si by 3M Scotch tape, and a few-layer h-BN flake was transferred on a transparent PDMS film with a similar method. Under the help of an optical microscope, the h-BN flake was aligned on the MoS_2 as designed. After a slight press, the h-BN was transferred on the desired position due to the affinity difference between the PDMS and SiO_2. A few-layer BP flake was aligned on the obtained h-BN/MoS_2 heterostructure with the similar method. Through this method, a BP/h-BN/MoS_2 heterostructure was formed. In the end, EBL was employed to define Au/Cr (50 nm/5 nm) electrodes on the produced BP/h-BN/MoS_2 heterostructure.

Device Characterizations: Keithley 4200-SCS semiconductor analyzer was employed to characterize the electrical properties of the devices in a probe station with a vacuum of 10^{-4} Pa. AFM (Bruker Dimension Edge) was used to determine the thickness of BP, MoS_2, and h-BN flakes under a tapping mode. Raman measurement was carried out with a Horiba Jobin Yvon LabRAM HR Raman system. The excitation was provided by a 514 nm laser with a power of 5 mW.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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